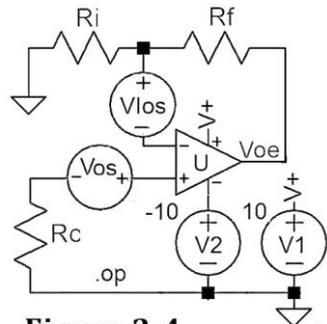


## Simulation: Offset Voltage and Offset Current

The *LTspice* “Opamps” library contains *Linear Technology* op-amp models, an ideal op-amp (opamp), and a generic non-ideal op-amp (UniversalOpamp2). The op-amp models in the *LTspice* library have their offset voltages and offset currents set to zero. Their bias currents are usually set to their typical data-book value.

One can refer to a particular op-amp’s datasheet to determine the range of its input offset current and input offset voltage. The maximum output offset voltage error for an op-amp circuit can be calculated from this data.

When using the *LTspice* models, the offset voltages and currents can be added external to the model as shown in figure 2-4 on the right. The effect of an offset current is modeled by adding a voltage source in series with the op-amp’s inverting terminal. The value of the voltage is equal to the additional voltage that would be produced by the offset current across the parallel combination of  $R_i$  and  $R_f$ .



**Figure 2-4**

$$V_{Ios} = \frac{R_i R_f}{R_i + R_f} I_{os}$$

A positive value of  $V_{Ios}$  will result in a positive change of the output voltage,  $V_{oe}$ . A positive value of  $V_{os}$  will result in a positive change of the output voltage,  $V_{oe}$ .

It’s easy enough to calculate the effect of an offset voltage or offset current in a particular circuit. The *LTspice* circuit in figure 2=4 above can be used to check calculated results. Refer to the example below.

### Example Results: LT1013

A *Linear Technology* LT1013 was used in the circuit of figure 2-4. Simulations were run for various resistor values, input offset voltages, and input offset currents. The LT1013’s offset voltage was determined by setting  $R_i$ ,  $R_c$ ,  $V_{Ios}$  and  $V_{os}$  to zero.

For this simulation  $R_i$  and  $R_c$  were actually set to  $1\mu\Omega$  so that they would still appear on the schematic and in the operating point analysis.

LTspice analysis results are given in the table below.

|   | Rf=2k except in last row Rf=2M                            | Voe   | I(Ri) | I(Rc) | I(Rf)  |
|---|---|-------|-------|-------|--------|
| 1 | Ri=Rc=1μ, Vios=0, Vos=0                                   | -25pV | 12nA  | 12nA  | -.13fA |
| 2 | Ri=2k, Rc=1K, Vios=0, Vos=0                               | 12pV  | 6nA   | 12nA  | -6nA   |
| 3 | Ri=2k, Rc=1K, Vios=0, Vos=50m                             | 100mV | 25μA* | 12nA  | -25μA* |
| 4 | Ri=2k, Rc=1K, Vios=8μ, Vos=0                              | 16μV  | 10nA  | 12nA  | -2nA   |
| 5 | Ri=2M, Rc=1M, Vios=8m, Vos=0                              | 16mV  | 10nA  | 12nA  | -2nA   |
|   | *I(Ri) = 25006nA, *I(Rf) = -24994nA, I(Ri) - I(Rf) = 12nA |       |       |       |        |

Row 1: The LT1013's input offset voltage is zero because the output voltage, Voe, is essentially zero (-25 X 10<sup>-12</sup> volts). There can be no output voltage error due to bias currents because both inputs are connected to ground (through 1μΩ resistors).

Row 2: The LT1013's non-inverting input's bias current is 12nA as indicated by I(Rc). Ri and Rf each have a current of 6nA. Both of these currents flow into the LT1013's inverting input. So both inputs have the same bias current indicating that the offset current is zero. Since the value of Rc is equal to the value of the parallel combination of Ri and Rf, the output offset error voltage, Voe, is essentially zero.

Row 3: An input offset voltage of 50mV produces an output error voltage of 100mV. Note that the bias currents are still 12nA. The theoretical output error voltage is calculated below.

$$V_{oe} = V_{os} \left( \frac{R_i + R_f}{R_i} \right) = 50\text{mV} \left( \frac{2\text{k} + 2\text{k}}{2\text{k}} \right) = 100\text{mV}.$$

Row 4: An input offset current of 8nA (represented by Vios = 8μV) produces an output error voltage of 16μV.

$$V_{ios} = \frac{R_i R_f}{R_i + R_f} I_{os} = (1\text{k})(8\text{nA}) = 8\mu\text{V}.$$

Row 5: If all the resistor values are increased by a factor of 1000, the output offset voltage also increases by a factor of 1000. The theoretical output error voltage is calculated below.

$$V_{oe} = R_c (I_{b-} - I_{b+}) \left( \frac{R_i + R_f}{R_i} \right) = (1 \times 10^6) (8 \times 10^{-9}) 2 = 16\text{mV}.$$

## Simulation: Op-Amp Noise

Spice op-amp models will usually have typical data sheet noise values.

The LT1013 data sheet specifies the op-amp's equivalent input noise voltage,  $V_{NI}$ , at 10Hz as 24nV/√Hz. Its equivalent input noise current,  $I_N$ , at 10 Hz is 0.07pA/√Hz. These values are per unity square root bandwidth.

|                    |          |
|--------------------|----------|
| Output:            | V(Vo)    |
| Input:             | V1       |
| Type of Sweep:     | Decade ▾ |
| points per decade: | 10       |
| Start Frequency:   | 10       |
| Stop Frequency:    | 1meg     |

An op-amp model's equivalent input noise voltage can be determined by performing a noise simulation on a voltage follower (buffer) circuit.

The circuit in figure 2-5 is simulated. Select the "Edit Simulation Cmd". Select "Noise". The dialog box shown on the left appears.

```
.noise V(Vo) V1 dec 10 10 1meg
```

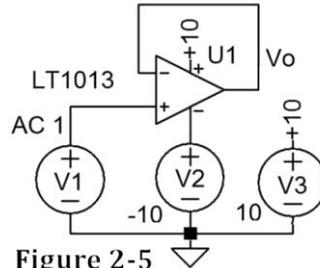
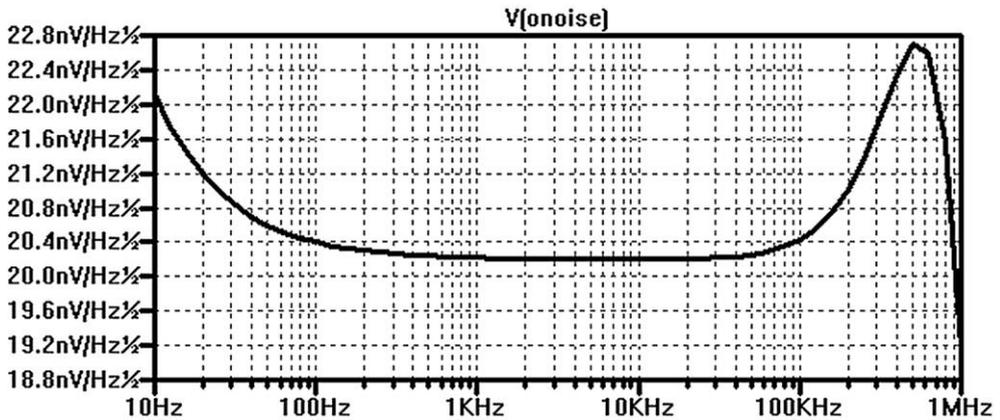


Figure 2-5

The noise simulation settings for this example are shown above and the simulation result is shown below.

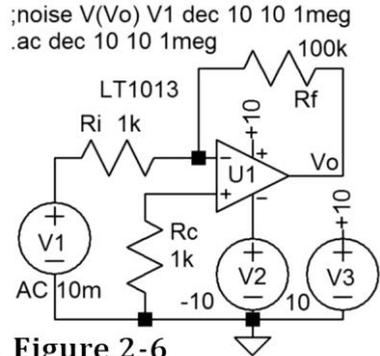


The noise simulation result above shows 22nV/√Hz at 10Hz which is close to the data sheet value of 24nV/√Hz.

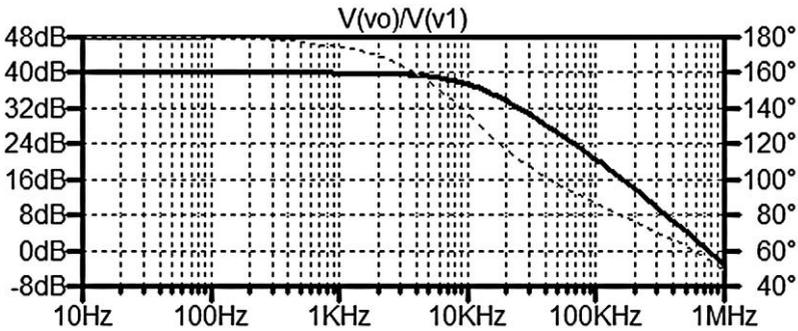
## Simulation: Frequency Response and Noise

Figure 2-6 on the right shows an inverting amplifier with a gain of 100. Since the gain-bandwidth-product of the LT1013 is 1MHz, its cutoff frequency is about 10KHz.

First, the frequency response of the amplifier will be simulated. Select “*Edit Simulation Command*” and “*AC Analysis*”. Set type of sweep to decade, points per decade to 10, start frequency to 10, and stop frequency to 1meg. The result is shown below. The dashed line is the phase response.

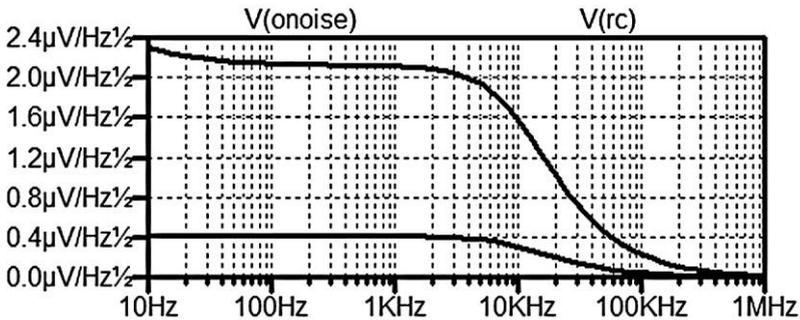


**Figure 2-6**



AC analysis frequency response plot verifies the expected cutoff frequency of 10KHz. It also shows that the unity gain frequency is 100KHz and that the circuit’s phase margin is about 55 degrees.

Next, the noise of the amplifier will be simulated. Select “*Edit Simulation Command*” and “*Noise*”. Set the output to V(Vo), input to V1, type of sweep to decade, start frequency to 10, and stop frequency to 1meg. A graph of the simulation results is shown below.



The plot above shows the total noise and the noise for the resistor, Rc.

### Calculated noise

Resistor thermal noise:  $1k = 4.07nV/\sqrt{Hz}$ ,  $100k = 40.7nV/\sqrt{Hz}$ .  
 Resistor current noise:  $1k = .07nV/\sqrt{Hz}$ . Current noise is negligible.  
 Total noise,  $V_{NI}$ :

$$V_{NI} = \sqrt{(22nV)^2 + (4.07nV)^2 + (4.07nV)^2 (.99)^2 + (40.7nV)^2 (.0099)^2}$$

$$V_{NI} = 22.74nV, \quad V_{No} = 22.74nV(101) = 2.3\mu V.$$

### Simulation: Transient Response

Transient analysis is used to display circuit voltages and currents in the time-domain. The voltage source V1 in figure 2-7 on the right is set by right clicking on it. V1 is set to produce a 400mV, 1KHz sine wave as shown below.

Functions

- (none)
- PULSE(V1 V2 Tdelay Trise Tfall Ton Period Ncycles)
- SINE(Voffset Vamp Freq Td Theta Phi Ncycles)
- EXP(V1 V2 Td1 Tau1 Td2 Tau2)
- SFFM(Voff Vamp Fcar MDI Fsig)
- PWL(t1 v1 t2 v2...)
- PWL FILE:

|               |      |
|---------------|------|
| DC offset[V]: | 0    |
| Amplitude[V]: | 400m |
| Freq[Hz]:     | 1k   |
| Tdelay[s]:    | 0    |
| Theta[1/s]:   | 0    |
| Phi[deg]:     | 0    |
| Ncycles:      | 2.5  |

SINE(0 400m 1k 0 0 0 2.5) .tran 2.5m

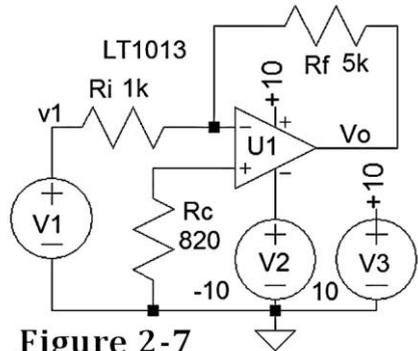
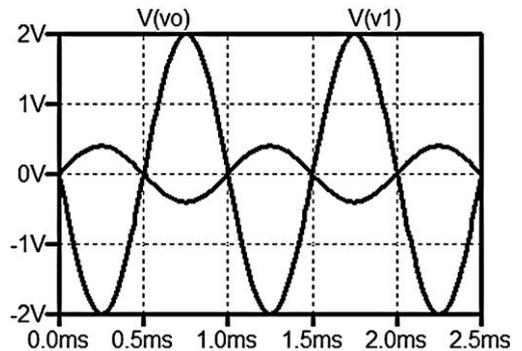


Figure 2-7

Two and a half cycles of the input and output wave forms are show in the result of the simulation below.



This is a gain 5 inverting amplifier.  $V_o$  is 5 times  $V_1$  and  $180^\circ$  out of phase.